**Enrollment No:** _____ **Exam Seat No:** _____

# C.U.SHAH UNIVERSITY

## Summer Examination-2018

**Subject Name : VLSI Technologies**

**Subject Code : 4TE08VLS1** **Branch: B.Tech (EEE)**

**Semester : 8** **Date : 01/05/2018** **Time : 02:30 To 05:30** **Marks : 70**

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

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**Q-1** **Attempt the following questions:** **(14)**

**a)** Which of the materials is used as gate? 01

A) Photoresistive B) Polysilicon C) Metal D) Glass

**b)** The _____ of the VLSI chip ranges from pre-assembly wafer preparation to fabrication techniques for the packages that provide electrical connections and mechanical and environmental protection. 01

A) Placement B) Floor-planning C) Packaging D) None

**c)** When a MOS transistor has conducting channel region at zero gate bias then it is called _____. 01

A) Depletion mode B) Enhancement mode

C) Saturated mode D) Non- saturated mode

**d)** If packing density area and performance are the constraints, power dissipation is not a constraint, the technology you prefer. 01

A) BJT B) CMOS C) NMOS D) PMOS

**e)** The value of VGS that makes ID approximately zero is the _____. 01

A) Pinch-off voltage B) Cutt-off voltage C) Ohmic D) Breakdown voltage

**f)** Using a hardware solution for a digital system is always _____ than a software solution. 01

A) Slower B) Harder C) Easier D) Faster

**g)** The final step in a design flow in which the logic design is implemented in the target device is called _____. 01

A) Design entry B) Simulation C) Downloading D) Compiling

**h)** _____ is ideally suited for applications using battery power or battery backup power. 01

A) N-MOS B) P-MOS C) CMOS D) MOS

**i)** The time needed for an output to change as the result of an input change is known as _____. 01

A) Noise immunity B) Fan-out C) Rise time D) Propagation delay

**j)** _____ is a light sensitive organic polymer. 01

A) Photoresist B) N-channel C) P-channel D) None of these

**k)** Which of the following is/are the operating mode(s) of a MOS transistor? 01

A) Accumulation mode only B) Depletion mode only
C) Inversion mode only D) All of the above

**l)** Which of the following is/are the region(s) of operation of a MOS transistor? 01

A) Cut-off region only B) Saturated region only
C) Non-saturated region only D) All of the above

**m)** NMOS technology is preferred more than PMOS technology due to _____. 01

A) High switching speed B) Low power consumption
C) Low cost of fabrication D) None of these

**n)** In CMOS fabrication, nMOS and pMOS are integrated in same substrate. 01

A) True B) False

**Attempt any four questions from Q-2 to Q-8**

**Q-2 Attempt all questions** **(14)**

**a)** Write a technical note on MOSFET capacitance. 07

**b)** Explain the design hierarchy of VLSI technology. 07

**Q-3 Attempt all questions** **(14)**

**a)** Write technical note on CMOS n-Well process. 07

**b)** Explain VLSI Design flow using Y-chart. 07

**Q-4 Attempt all questions** **(14)**

**a)** Explain briefly VLSI design methodology. 07

**b)** Explain the construction & working of a CMOS transistor. 07

**Q-5 Attempt all questions** **(14)**

**a)** Explain the differences between NMos & PMos. 07

**b)** Discuss CMOS SR latch circuits based on NOR2 gates. 07

**Q-6** **Attempt all questions** **(14)**

**a)** Draw the circuit diagram of a CMOS edge-triggered D-latch and explain. 07

**b)** Explain the differences between AOI and OAI. 07

**Q-7** **Attempt all questions** **(14)**

**a)** Give comparison between FPGA and CPLD. 07

**b)** Write a note on Built-In Self-Test (BIST). 07

**Q-8** **Attempt all questions** **(14)**

**a)** Explain CMOS dynamic circuit techniques. 07

**b)** Explain the basic principle of pass transistor circuit. Explain logic“1” transfer and logic “0” transfer. 07